

Differential Ring Voltage Controlled Oscillator -A Review

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Abstract— A review on some of the differential ring voltage- controlled oscillators (VCO) designs has been presented in this paper. Various differential delay cells have been studied and a comparison has been made in terms of oscillation frequency, power consumption and phase noise.

Keywords—dual-delay path, phase noise, voltage-controlled oscillator (VCO).

I. INTRODUCTION

Voltage controlled oscillators (VCOs) are the electronic circuits which are used for high speed clock generation, channel selection, frequency modulation and demodulation in various communication circuits. In the modern communication systems, there is a calculated gap between the adjacent channels for the efficient use of frequency spectrum. Therefore, in order to avoid interference and noise problems, the characteristics of an oscillator are of much importance. Among the compilation of signals, oscillator must be able to detect the desired signal. Hence VCO is a critical component of frequency synthesizer circuits and PLLs. The performance parameters for VCO includes 1) Wide frequency tuning band 2) Low phase noise 3) Low power supply noise 4) Less power dissipation at low supply voltage and small scale technology. Therefore, many research have been done in this field. Two widely used VCOs are 1) LC oscillators and 2) Ring VCOs. LC oscillators have better phase noise performance than ring oscillators but the latest trends demand the design with easy implementation of the circuit, small chip area, low cost and good performance. The implementation of high quality inductor and capacitor in a standard CMOS process requires extra non standard processing steps and also increases the chip area and the cost. On the other hand, ring oscillators are completely integrated circuits. Therefore, the next task is to improve the performance parameters for a ring VCO [2]-[6].

Like any oscillator, a VCO may be considered as an amplifier and a feedback loop. For the circuit to oscillate the total phase shift around the loop must be 360 degrees and the gain must be unity. In case of ring oscillators, the delay stages or cells are connected back to back. If there are N delay stages, the frequency of oscillation is given by $f = 1/2Nt_d$ where t_d is the delay of one delay cell. The less

number of delay cells with less propagation delay can increase the frequency of oscillation.

There are two kinds of ring VCOs: Single- ended and differential ring VCOs. The delay cell for the simplest single ended VCO is a basic inverter and has the highest frequency of oscillation and minimum power dissipation. To omit the need for by-pass and coupling capacitors, differential ring VCOs are more suited [1]-[4]. The dual loop technique in a differential VCO increases the oscillation frequency and also reduces the phase noise.

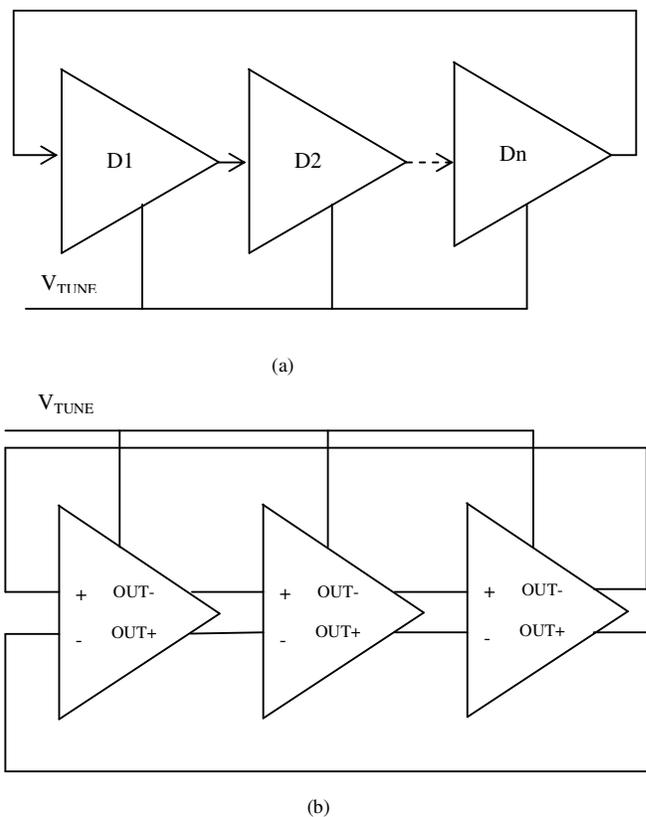


Fig.1. Block diagram (a) single- ended VCO (b) differential ring VCO.

II. TYPES OF DELAY CELLS

The schematic of the conventional delay cell [1] is shown in Fig. 2. Dual loop technique has been reported. In this circuit, NMOS transistors M1 and M2 form the primary loop, while the PMOS transistors M7 and M8 form the secondary loop. The primary inputs are fed from the outputs of the previous stage. The secondary inputs are fed from the outputs that are a few stages prior to the current stage. Output nodes will be pre-charged from M7 or M8. As a result, the output node can charge to a high voltage faster and hence increases the oscillation frequency. The PMOS load transistors M3 and M4 constitutes a latch. The strength of the latch also affects the oscillation frequency. The output oscillates from rail to rail because of latch and therefore, on- time of the transistors in the delay cell is reduced which further reduces the phase noise. The control voltage V_C at the gate of NMOS transistors M5 and M6 control the feedback strength of the latch.

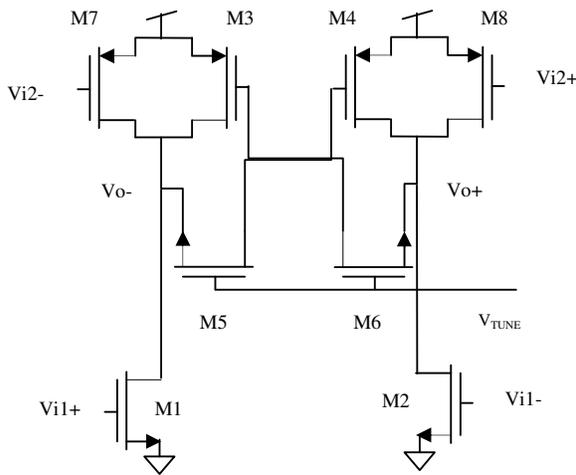


Fig. 2. Conventional delay cell [1].

As V_{TUNE} is increased, the latch becomes strong and hence resists the voltage switching in the delay cell. It increases the delay time of the differential delay cell and reduces the oscillation frequency. The tuning voltage range of this conventional delay cell is limited.

Another dual loop differential delay cell [2] is shown in Fig. 3. A pair of NMOS transistors M9 and M10 is added. These are used to pre- discharge the output nodes. As a result, the rise time and even the fall time of the output gets reduced which increases the oscillation frequency. The phase noise and supply noise of this delay cell is also lower than the conventional one as per the noise analysis [1] of fully switched ring oscillators. The generated noise power can be shown as

$$P_{noise} = \frac{\Delta T}{T} \frac{4kTR}{1+(2\pi f_m RC)^2} \quad (1)$$

where ΔT is the on-time of the transistors of the delay cell, T is

the oscillation period, f_m is the offset frequency from the carrier and RC is the time constant of the delay cell.

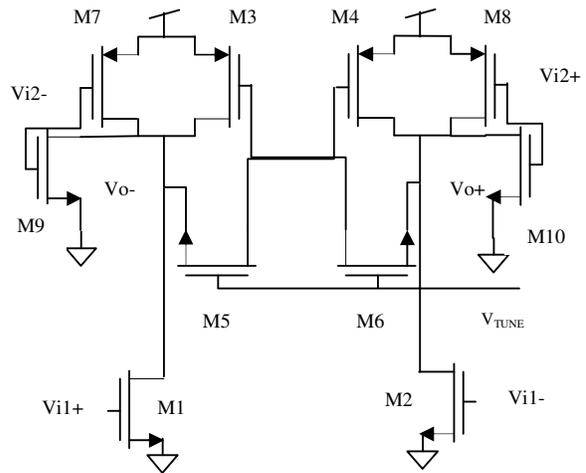


Fig. 3. Differential delay cell [2].

A 3-stage multi-loop ring oscillator has been reported in [3]. Multi-loop technique has been employed for the frequency boosting. As a result, the oscillator provides a high frequency of 7GHz. The circuit schematic is shown in Fig. 4. NMOS transistors N1 and N2 form the input pair of the primary loop while PMOS transistors P5 and P6 serve as inputs for the secondary loop. PMOS transistors P1 and P2 form the loads of the delay cell. When V_{p+} is lower than V_{tn} , N1 is in cut- off mode. Since the input voltage at V_{s+} is earlier than V_{p+} , P5 will already be conducting its source current to the load capac-

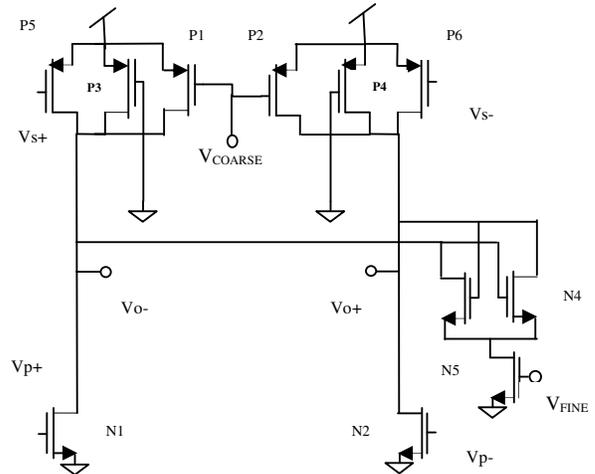


Fig. 4. Delay cell [3].

itor at the output node V_{o-} . As a result, the time for the output node to rise from low to high is decreased. In order to avoid the loss of oscillation at the extreme cases of frequency tuning, extra PMOS loads, P3 and P4, are added in parallel with the P1 and P2. In this design, the gates of P3 and P4 are connected to ground to bias the

transistors into the triode region of operation. Coarse tuning is accomplished by varying the load through changing the gate voltage of P1/P2. On the other hand, fine-tuning can be achieved by adjusting the amount of tail current flowing through the positive feedback latch, N3 and N4.

In order to achieve both wideband tuning and low K_{VCO} , switched capacitor array, has been introduced to the ring VCO in [4]. The schematic of the delay cell is presented in Fig. 5. C_1 and C_2 are the switched capacitors controlled by digital signals S1 and S2. The coarse frequency tuning is achieved by these switched capacitors. A lower K_{VCO} means less sensitivity to noise at the tuning node and the phase noise is improved.

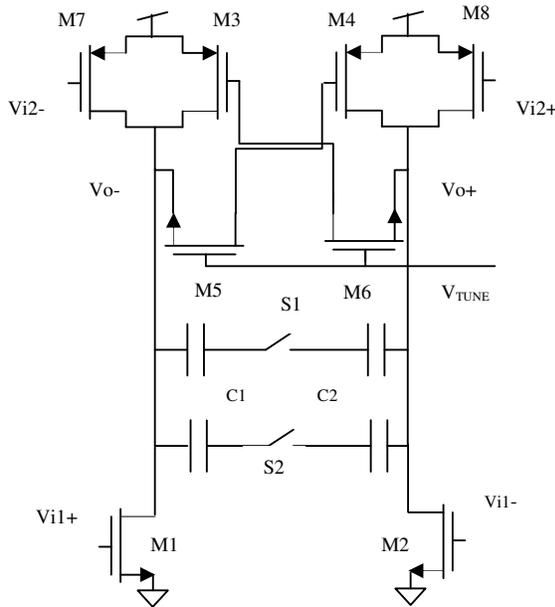


Fig. 5. Differential delay cell with SCR [4].

III. COMPARISON OF DELAY CELLS

Different differential delay cells have been studied in terms of different parameters like frequency, power dissipation and phase noise. These delay cells have been reported in various technologies ranging from 65 nm to 600 nm. Frequency ranges from 750 MHz to 1.2 GHz for four-stage ring VCO [1]. Power dissipation for this oscillator is 30 mW and phase noise is -117 dBc/Hz at an offset of 600 KHz. Further, a four- stage ring VCO with delay cell [2] gives oscillation frequency in the range of 850 MHz to 2.1 GHz. Power consumption is 10.2 mW at 1.5 GHz for this circuit. Moreover, three stage ring oscillator [3] results in a very high oscillation frequency ranging from 7.3 GHz to 7.68 GHz. This circuit consumes a very high power of 60mW. Phase noise for this VCO is -103.4 dBc/Hz at an offset of 1 MHz from the carrier frequency. Finally, a ring VCO with four stage delay cell [4] results in a very small power dissipation of 3.84 mW.

Frequency range is 480MHz to 1.1 GHz and phase noise is -120 to -108 dBc/Hz at 1MHz offset. Table 1 lists the comparison of various differential delay cells.

TABLE I. COMPARISON OF DIFFERENT DELAY CELLS

| Delay cell | Technology | Frequency (MHz) | Power (mW) | Phase noise (dBc/Hz) |
|------------|------------|-----------------|--------------|----------------------|
| [1] | 600nm | 750-1200 | 30 | -117@600 KHz |
| [2] | 250nm | 850-2100 | 10.2@1.5 GHz | - |
| [3] | 130nm | 7300-7860 | 60 | -103.4@1 MHz |
| [4] | 65nm | 480-1100 | 3.84 | -120 to -108@1 MHz |

IV. CONCLUSION

Four different delay cells have been studied and compared in terms of frequency of oscillation, power dissipation and phase noise. Ring oscillators provide a wide range of frequency components. These dual delay cells have the advantages of lower power consumption with lower phase noise. It has been observed that dual delay cells are very stable cells for designing ring based oscillators. These observations are based on different technology parameters.

REFERENCES

- [1] C.H.Park and B.Kim, "A low noise ,900 MHz VCO in 0.6- μ m CMOS," IEEE J.Solid- State Circuits, vol. 34,no. 5, pp. 586-591, May 1999.
- [2] K.H.Cheng, S.C.Kuo and C.M.Tu, "A low noise ,2.0 GHz CMOS VCO design," IEEE Symposium on Circuits and Systems, vol. 1, pp. 205-208, Dec. 2003.
- [3] H.Q.Liu, W.L.Goh, L.Siek, et al, "A- low noise multi- GHz CMOS multiloop ring oscillator with coarse and fine frequency tuning," IEEE Transactions on VLSI Systems, vol.17,no. 4,pp. 571-577, April 2009.
- [4] G.Haijun, S.Lingling, et al, "A low- phase- noise ring oscillator with coarse and fine tuning in a standard CMOS process," IOP Science Journal of Semiconductors, vol. 33,no. 7, July 2012.
- [5] M.Kumar, S.K.Arya and S.Pandey, "A low power voltage controlled ring oscillator design with substrate biasing," International Journal of Information and Electronics Engineering, vol. 2,no. 2, March 2012.
- [6] M.Kumar, S.K.Arya and S.Pandey, "A low power voltage controlled ring oscillator design with novel 3 transistors XNOR/XOR gates," Circuit and Systems Journal, USA, vol. 2,no. 3, pp. 190-195, July 2011.