Analysis of Single-Event Upsets in Phase-Locked Loops

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Abstract—**Exploration of space provides us with useful information about the universe. Understanding the number of issues and solving them lead to progress in this field. The sun is major source of radiation, thus the radiation experienced by the space-craft in the outer space is one of the issue. The electronic circuitry on-board the space-crafts are exposed to these radiations and may result in reduction of the lifetime of the space-crafts and even cause failure. Thus for successful and safe exploration of space it is necessary to analyze and understand the effects of radiation on any electronics circuitry. One of the main integral parts of many electronic systems is a phase-locked loop(PLL) which is widely used in commercial and space-deployed electronic system to reduce phase delay associated with distribution of clock signal. Single event upsets (SEUs) have been a growing concern in modern integrated circuits (ICs) where increased susceptibilities to SEUs have been reported as device feature sizes decrease and operating frequencies increase [1]. Thus analyzing the effects of single event transients (SET) in PLL is important for all these applications. This paper summarizes effects of radiation on different blocks in PLL.**

Keywords- Phase-locked loop; Single event effect; Single event transien; Single event upset.

I. INTRODUCTION

Phase-locked loops (sometimes termed bit synchronization circuits, or clock-recovery circuits) are widely used in many commercial and space-deployed electronics systems, to minimize the phase delay associated with the distribution of clock signals. It is also used for number of applications such as local oscillator in wireless communication system, clock recovery circuitry at serial or parallel high speed data links, synchronizing data transmission and as a frequency synthesizer in digital systems. Current work with computer circuit-level simulation techniques has enabled the understanding of single event upset (SEU) [1, 2] in mixed-signal applications such as the phase-locked loops (PLLs). In space deployed electronics, PLLs circuits have been identified as more prone to single event upsets, thus there is a growing interest on the SEU impacts in the PLL.

The basic structure analysis of the phase-locked loop is introduced by [3, 4].Here we introduce a current source to the simulations which are able to produce the same effect as that of a heavy ion or laser strike and the sensitivity of the circuit to SET effects is observed.

II. DESCRIPTION

A block diagram of Generic Phase-Locked Loop (PLL) is shown in Fig. 1.

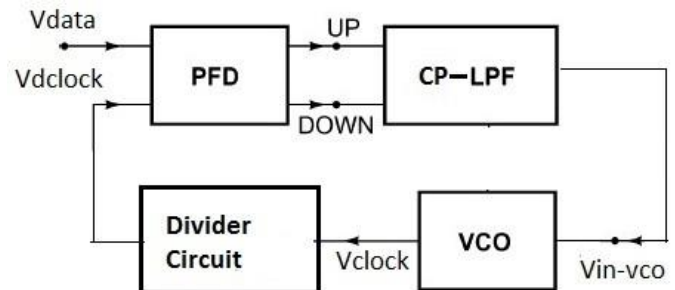


Fig. 1: A Generic Phase-Locked loop.[5]

The PLL [4, 5] is used to create a stable output signal that is synchronized to an input reference signal. The input reference signal to the phase locked loop circuit may be a digital clock signal or data received from a transmission network. Thus, in steady-state, the difference between the input and output phases should not be changing over time; that is, the output phase of the PLL should be “in lock" with the phase of the input reference signal. Also a phase-locked loop able to track an input frequency, or it can generate a frequency that is a multiple of the input frequency. Phase-locked loops are widely employed in applications such as modulators /demodulators in wireless communication, as a frequency synthesizers, synchronizers and multiplexers [6, 7].

The basic building blocks of a phase-locked loop are, phase frequency detector(PFD), low pass filter(LPF), voltage-controlled oscillator(VCO) and divider circuit. Every PLL design has these modules tailored to achieve specific performance and obtain stability requirements for a particular range of operating frequencies. Here each of these blocks is discussed below.

A. *Phase Frequency Detector (PFD)*

The phase frequency detector in a phase-locked loop circuit generates a difference signal (error signal) which is some function of the phase difference (phase error) between the feedback signal to that of the reference signal. The phase frequency detector (PFD) generates an output signal

proportional to the time difference between input signal 'Vdata' and the divided down clock signal 'Vdclock'. Figure 2 illustrates the typical CMOS implementation of the PFD using inverters and NAND gates.

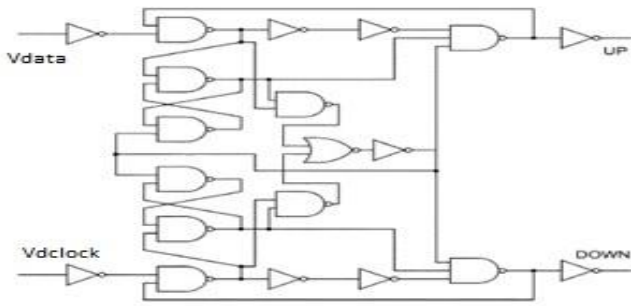


Fig. 2: Circuit schematic of the phase-frequency detector (PFD)[6]

The PFD functions by sensing the transitions occurring in the 'Vdata' and 'Vdclock' signals, detecting the phase and frequency differences between their rising edges, and giving pairs of (UP, DOWN) signals at the output accordingly. Figure 3 illustrates the output of PFD block in PLL analyzed without current pulse strike(I_{SEU}).

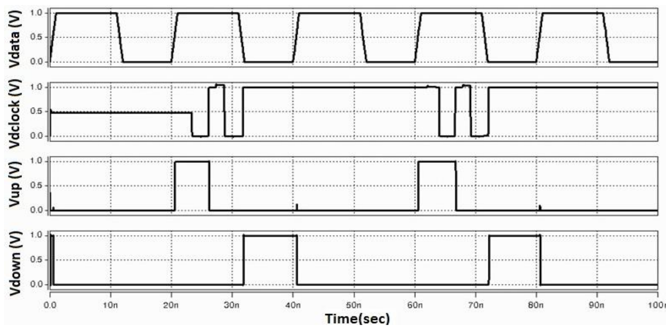
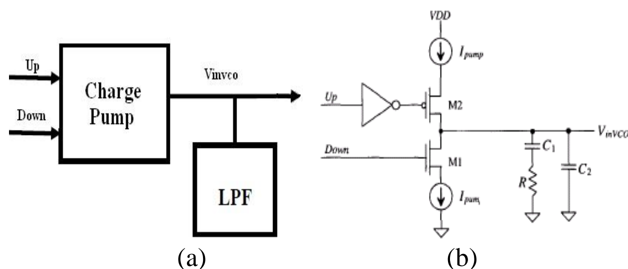


Fig. 3: Simulation result of PFD without an effect of current strike(I_{SEU}).

B. Charge-Pump and Low pass filter (CP-LPF)[8]

There are different configurations of Low Pass Filter such as the tri-state LPF and the charge-pump LPF. The output stage of charge pump supplies current to the loop filter that generates the control voltage for frequency operation of the voltage-controlled oscillator block (VCO) [9]. Figure 4 shows charge pump (CP)-Low Pass Filter (LPF) block diagram and circuit diagram respectively.



(a) (b)

Fig. 4: Charge Pump-LPF[6]
a) Block diagram b) Circuit diagram

The UP signal is high when the input reference signal is operating at a higher frequency than the feedback signal and thus the charge-pump forces current into the loop filter. This causes the VCO control voltage to increase and thus increases the VCO frequency and brings the feedback frequency to move towards the input reference signal.

Similarly, the DOWN signal is high when the feedback signal is operating at a higher frequency than the input reference signal and thus the charge-pump sinks current out of the loop filter. This causes the VCO control voltage to decrease and thus decreases the VCO frequency and brings the feedback frequency to match with the input reference signal. The loop filter is used to integrate the current pulses that flow from/to the charge-pump and convert them to voltages[10].

Figure 5 shows simulation of Charge-pump and low pass filter without current pulse (I_{SEU}) strike.

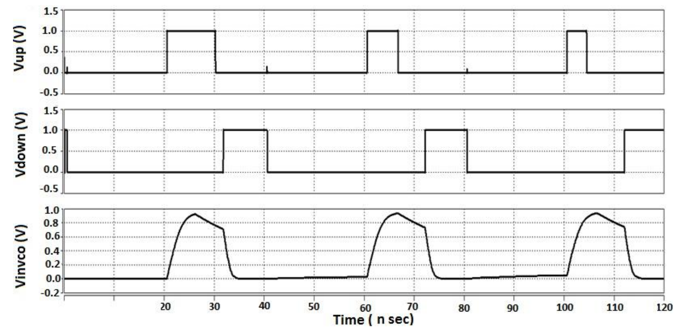


Fig. 5: Simulation Result of CP-LPF without an effect of current strike(I_{SEU}).

The signals UP and DOWN which are obtained as output in PFD block are fed as an input to the charge pump-low pass filter block in PLL. The output signal (Vinvco) is as shown in fig. 5.

C. Voltage-Controlled Oscillator

Voltage-controlled oscillator is a block, which generates the signal with required frequency for the PLL. The VCO is a circuit, which can tune the oscillator output frequency from the control voltage [8,11]. The voltage at the input of the VCO changes with every clock cycle as the PFD continues to compare the leading edges of the signals Vdata and Vdclock, and the charge-pump module continues to source or sink current to or from the LPF.

Figure 14 shows simulation of VCO without an effect of current (I_{SEU}) strike. The analysis of input signal Vinvco and output signal Vclock in VCO component of PLL is as shown in fig. 6.

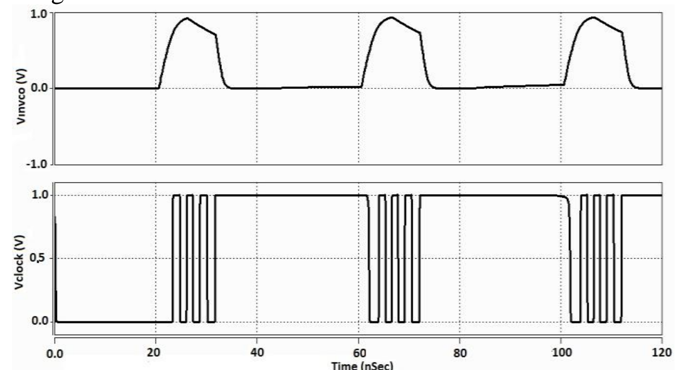


Fig. 6: Simulation result of VCO without an effect of current strike(I_{SEU}).

D. Divider Circuit

The feedback path is often employed as a sequence of frequency dividers. It divides the higher output frequency by a multiplication factor N to match the reference frequency [12]. Figure 7 shows the simulation result of divider block without an effect of current (I_{SEU}) strike. Figure 7 shows the simulated waveforms for input signal Vclock and output signal Vdclock in divider block of PLL.

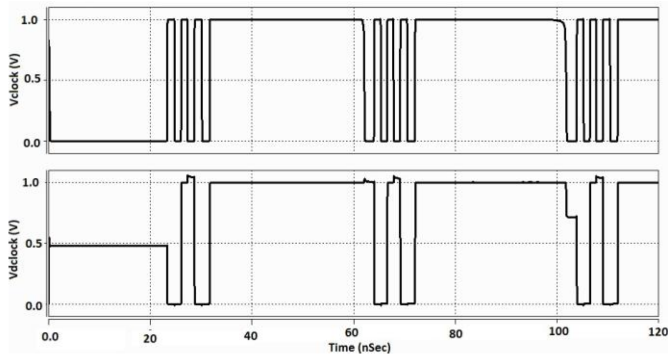


Fig. 7: Simulation result of divider block without an effect of current strike(I_{SEU}).

III. Single Event Upset

A single-event effect (SEE) occurs when a high energy ionizing particle, such as a heavy ion, bombards with the circuit. These excess carriers generated gets collected on circuit nodes and thus result in undesirable circuit responses which can vary depending on the structure of the circuit, the amount of charge deposited as well as collected on the particular circuit node. One type of effect resulting from single event effect in an IC is a single event transient (SET). In digital circuits, an SET can result in a single-event upset (SEU), that is, an alteration of the state of memory circuits. Heavy ion strike due to ionizing radiation is the main reason for generation of SET effects in an electronic circuitry. When radiation strike occurs, SET propagates through the subsystem and reaches a circuit node where it can trigger a change [1, 2].

The SET effect can lead to a circuit error if the erroneous/corrupted data moves throughout the circuit. Experimentally SET effect can be studied using circuit simulation [13]. Even though circuit simulation requires large time period, it is the best way to study the factors that get affected due to SET [14].

IV. Simulation And Results

The effect of SEU on PLL circuit can be studied by introducing a current source at a critical node in the PLL circuit which will have the same effect on PLL circuit as that of the laser strike or a heavy-ion strike, which produces SET effect in electronic circuitry [14].

Therefore in circuit simulation, the charge deposition at a particular node in a circuit where radiation hit occurs is shown by a current source (I_{SEU}) as shown in fig 8. The current spikes are generated using an exponential function with 100mA amplitude (at 22nsec) and analyzed the effect of current spike on transient response. This current is integrated to find value of the charge at that particular node. Thus 100mA current spikes deposit the charge 9.1234 pC at the Vinvco node and change the output of PLL permanently.

Table.I: Amount of charge induced by Current spike of 100mA amplitude at the critical node Vinvco.

Amplitude of a current pulse (I_{SEU})	Charge induced (Q)
100mA	9.1234pC

If the current induced by the strike is large enough then the respective transistor cannot balance the current and thus voltage change occurs at that node and brings significant variation in the circuit output. Figure 8 shows representation of laser pulse at Vinvco node of PLL at 22ns.

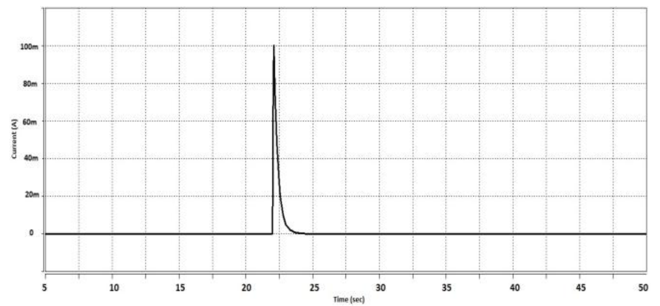


Fig. 8. Current spike generated by the current source of 100mA at 22nsec.

Simulation is carried out using bulk-45nm PTM technology model files. A current source with value 100mA has been inserted at the output of charge pump-low pass filter which is an input to the voltage-controlled oscillator block i.e. Vinvco node of the complete PLL circuit and analyzed its effect on the PLL circuit. Pulse model is used as an input with pulse width of 20nSec and the current pulse is struck at the drain of NMOS transistor M1 and observed the initial changes in the output response.

The input signal (data) and feedback signal (dclock) simulated under the effect of radiation i.e. a current pulse (I_{SEU}) strike in PFD component of PLL. Figure 9 shows the output response of PFD block where feedback signal Vdclock undergoes a phase shift as compared to the PFD block simulated without any current strike shown in fig. 3 above.

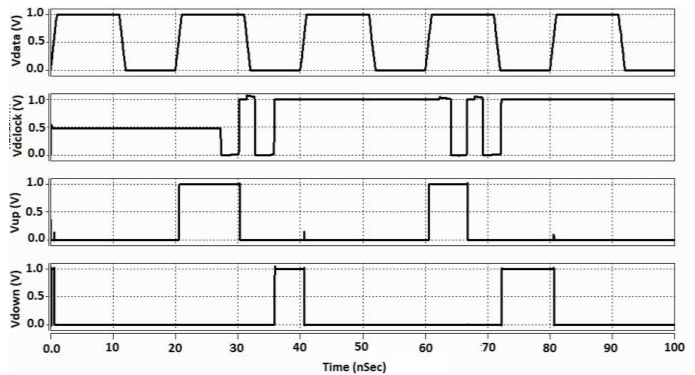


Fig. 9: Simulation result of PFD with current pulse (I_{SEU}) strike.

Similarly the simulation results of different blocks such as Charge pump-low pass filter(CP-LPF), voltage-controlled oscillator(VCO) and divider circuit under the effect of current pulse (I_{SEU}) striking at Vinvco node in PLL circuit are as shown in fig. 10.

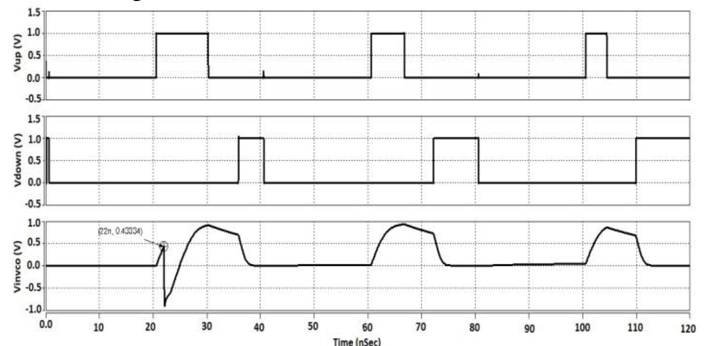


Fig. 10: Simulation Result of CP-LPF under the effect of current pulse (I_{SEU}) at 22ns.

The output of Charge pump-LPF block i.e. Vinvco which would be high without the spike, undergoes a negative transition but retains its original value after a specific amount

of time as shown in fig. 10.

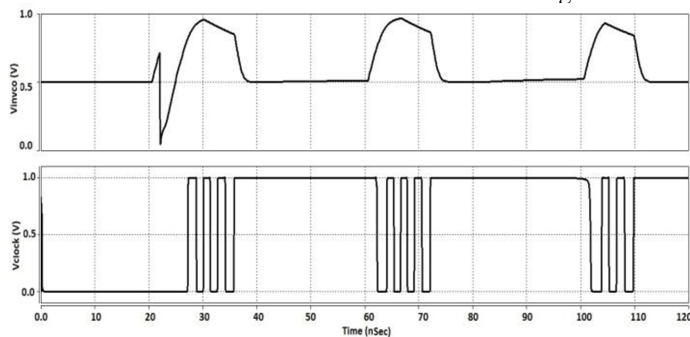


Fig. 11: Simulation result of VCO under the effect of current pulse (I_{SEU}) at 22ns.

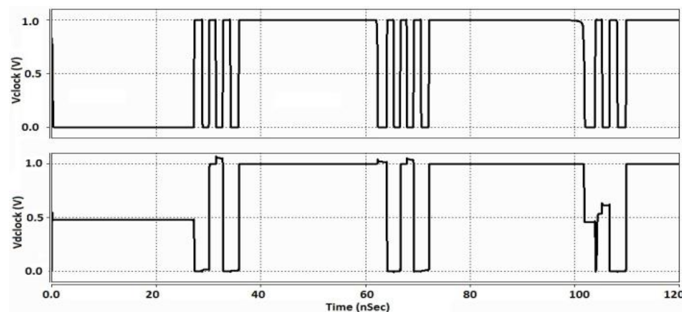


Fig. 12: Simulation result of Divider block under the effect of current pulse (I_{SEU}) at 22ns.

Finally the simulation results with and without a current pulse (I_{SEU}) strike for complete PLL circuits are shown in the fig. 13.

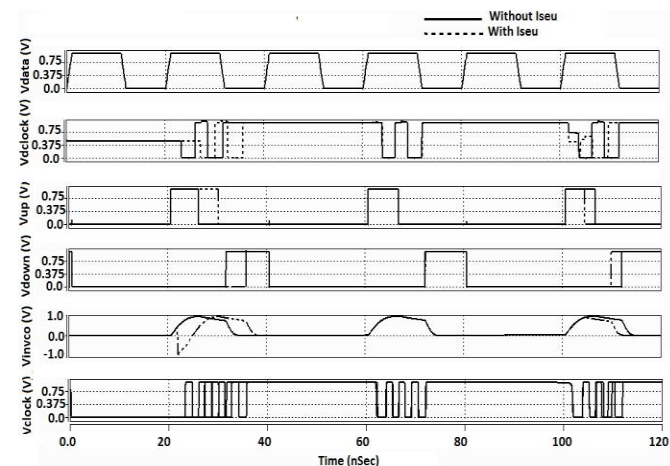


Fig. 13: Simulation Result for complete PLL with and without current pulse (I_{SEU}) strike at 22ns.

The solid lines represents output waveforms for a phase locked loop without any radiation effect (current strike), whereas the dotted lines represents output waveforms with current pulse (I_{SEU}) striking at 22nsec at Vinvco node in PLL. The waveforms with current pulse inserted at 22nsec clearly show shift in phase due to the current strike which may cause the system failure if current induced is high.

V. FUTURE WORK

This work study effects of radiation on different blocks in a phase locked loops using simulation software at 45nm. Since phase locked loops have been identified as single event (SE) vulnerable circuits in space deployed electronics circuitry, it is necessary to mitigate the effect of radiation by applying different radiation hardening techniques. Future work includes efficient radiation hardening method for PLL to minimize these radiation effects with minimum impact on circuit design.

VI. CONCLUSION

In this paper we analyzed the PLL circuit by applying a current pulse across the junction more vulnerable to current induced upsets. The characteristics of phase-locked loop get affected due to the induced current pulse. From the analysis and simulation done above, it is observed that, single event upsets generated in any electronics circuit can easily disturb its output response even if amplitude of current pulse is small.

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